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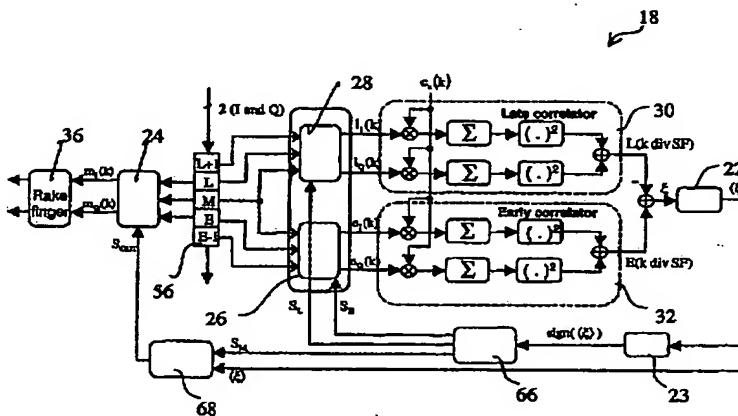
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(54) Title: EARLY-LATE SYNCHRONIZER HAVING REDUCED TIMING JITTER



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(57) **Abstract:** A device for maintaining fine alignment between an incoming spread spectrum signal and a locally generated code in a digital communication receiver comprises: - a delay line (56) for storing a plurality of consecutive samples (E-1, E, M, L, L+1) of the incoming spread spectrum signal; - three digitally controlled interpolators (24, 26, 28) for determining by interpolation between consecutive samples an interpolated early sample (e), an interpolated middle sample (m) and an interpolated late sample (l); - two correlators (30, 32) for calculating an error signal (ξ) as the difference between the energy of the symbols computed from the interpolated early (e) and late (l) samples; - a circuit for generating a control signal ($S_L OUT?$) for controlling the interpolation phase of the digitally controlled interpolator (24) for the early sample (e), and - a digital non-linear filter (68), for smoothing the control signal ($S_L OUT?$) of the interpolator (24) for the early sample (e), enabling the update operation of the control signal only when the absolute value ($|\xi(n)|$) of the error signal at a time instant n is smaller than the absolute value ($|\xi(n-1)|$) of the same error signal at a time instant n-1.

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